Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) [[The]] A universal serial bus device ~~in accordance with claim 1, wherein the interface comprises:~~ to be initialized as a state enabling a communication with a host, the host storing a real descriptor and a descriptor recognizing program, comprising:

an interface storing a predetermined basic descriptor, the interface primarily activating an initialization signal and transferring the basic descriptor to the host to perform a primary initialization, the interface downloading the real descriptor in response to a download command generated from the host, and secondarily activating the initialization signal and transferring the real descriptor to the host to perform a secondary initialization;

at least one signal line for guiding the basic descriptor, the real descriptor and the download command, the at least one signal line being enabled with a terminal voltage;

a voltage regulator providing the terminal voltage to the signal line while the initialization signal is activated;

a memory storing the basic descriptor;

a register for storing the real descriptor generated from the host;

a command analyzing portion receiving the real descriptor and the download command from the host and generating a download start signal; and

a descriptor read/write portion transferring the basic descriptor stored in the memory to the host, the descriptor read/write portion transferring the real descriptor outputted from the command analyzing portion to the register in response to the

download start signal and generating a download completion signal and providing the real descriptor stored in the register to the host.

3. (Original) The universal serial bus device in accordance with claim 2, wherein the interface further comprises:

a timer activating a control signal for controlling the activation of the initialization signal in response to the download completion signal; and

an initialization signal generator activating the initialization signal in response to the control signal.

4. (Original) The universal serial bus device in accordance with claim 3, wherein the control signal is primarily activated to terminate a primary activation of the initialization signal and is secondarily activated to generate a secondary activation of the initialization signal.

5. (Original) The universal serial bus device in accordance with claim 2, wherein the memory is a read only memory (ROM).

6. (Currently Amended) The universal serial bus device in accordance with claim [[1]] 2, wherein the voltage regulator comprises:

a transistor connected to a predetermined terminal voltage; and

a resistor being disposed between the transistor and the signal line.

7. (Original) The universal serial bus device in accordance with claim 3, wherein the voltage regulator comprises:

a transistor connected to a predetermined terminal voltage; and

a resistor being disposed between the transistor and the signal line..

8. (Original) The universal serial bus device in accordance with claim 7, wherein the transistor is controlled by the initialization signal generator.

9. (Canceled)

10. (Currently Amended) [[The]] A universal serial bus device ~~in accordance with claim 9, wherein the interface further includes:~~ to be initialized as a state enabling a communication with a host, the host storing a real descriptor and a descriptor recognizing program, comprising:

at least one signal line, connected to the host, for guiding data and commands, the at least one signal line being enabled with a terminal voltage;

an interface storing a predetermined basic descriptor, the interface primarily activating an initialization signal and transferring the basic descriptor to the host to perform a primary initialization, the interface downloading the real descriptor in response to a download command generated from the host, and secondarily activating the initialization signal and transferring the real descriptor to the host to perform a secondary initialization, the interface including a voltage regulator providing the terminal voltage to the signal line while the initialization signal is activated;

a memory storing the basic descriptor;

a register for storing the real descriptor generated from the host;

a command analyzing portion receiving the real descriptor and the download command from the host and generating a download start signal; and

a descriptor read/write portion transferring the basic descriptor stored in the memory to the host, the descriptor read/write portion transferring the real descriptor outputted from the command analyzing portion to the register in response to the download start signal and generating a download completion signal and providing the real descriptor stored in the register to the host.

11. (Original) The universal serial bus device in accordance with claim 10, wherein the interface further comprises:

a timer activating a control signal for controlling the activation of the initialization signal in response to the download completion signal; and

an initialization signal generator activating the initialization signal in response to the control signal.

12. (Original) The universal serial bus device in accordance with claim 11, wherein the control signal is primarily activated to terminate a primary activation of the initialization signal and is secondarily activated to generate a secondary activation of the initialization signal.

13. (Original) The universal serial bus device in accordance with claim 10, wherein the memory is a read only memory (ROM).

14. (Currently Amended) The universal serial bus device in accordance with claim [[9]] 10, wherein the voltage regulator comprises:

a transistor connected to a predetermined terminal voltage; and

a resistor being disposed between the transistor and the signal line.

15. (Original) The universal serial bus device in accordance with claim 11, wherein the voltage regulator comprises:

a transistor connected to a predetermined terminal voltage; and

a resistor being disposed between the transistor and the signal line.

16. (Original) The universal serial bus device in accordance with claim 15, wherein the transistor is controlled by the initialization signal generator.

17. (Canceled)

18. (Canceled)

19. (Canceled)